WHAT IS CLAIMED IS:

1. An integrated circuit comprising:

at least two logic circuits including a first logic circuit and a second logic circuit having the same function as said first logic circuit; and

a direction circuit for directing operation or halt of said first and second logic circuits,

wherein said direction circuit directs, in normal mode, the operation of one of said first and second logic circuits based on an externally supplied select signal, and directs, in testing mode, simultaneous operation of said first and second logic circuits when said select signal is a signal for selecting said first or second logic circuit.

2. The integrated circuit of Claim 1, further comprising:

a first output circuit for receiving an output of said first logic circuit;

a second output circuit for receiving an output of said second logic circuit; and

a signal line for receiving both the outputs of said first and second output circuits,

wherein said first and second output circuits enter an enable state in response to an externally supplied testing mode signal.

3. The integrated circuit of Claim 1,

wherein each of said first and second logic circuits performs a logic operation corresponding to a function according to an externally supplied function signal when the operation thereof is directed by said direction circuit.

4. A testing method for an integrated circuit composed of at least two logic circuits including a first logic circuit and a second logic circuit having the same function as said first logic circuit, comprising the steps of:

simultaneously operating said first and second logic circuits;

transferring outputs of said first and second logic circuits to one signal line;

measuring a supply current flowing through said signal line; and

determining whether said first and second logic circuits are defective or nondefective based on said measured supply current.